Express Mail Label No.

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
SEC.506

Total Pages in this Submission
3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT

and invented by:

Byoung-taek LEE
Ki-hoon LEE

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **26** pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. SEC.506
Total Pages in this Submission 3

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 8
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☒ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
    ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
SEC.506
Total Pages in this Submission
3

Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	20	- 20 =	0	x	$18.00	$0.00
Indep. Claims	2	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$760.00

☐ A check in the amount of to cover the filing fee is enclosed.

☐ The Commissioner is hereby authorized to charge and credit Deposit Account No. as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☐ Credit any overpayment.
- ☐ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Brian C Altmiller

Signature

Dated: **MARCH 26, 1999**

Brian C. Altmiller
Reg. No. 37,271

Jones, Volentine, Steinberg & Whitt, L.L.P.
12200 Sunrise Valley Drive, Suite 150
Reston, VA 20191

Tel. No. (703) 715-0870

cc:

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re Patent Application of

Byoung-taek LEE et al.

ATTN: APPLICATIONS BRANCH

Serial No. (NEW)

ATTORNEY DOCKET NO. SEC.506

Filed: March 26, 1999

For: METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT

CLAIM OF PRIORITY

Honorable Assistant Commissioner for Patents and Trademarks,
Washington, D.C. 20231

Sir:

Applicants in the above-identified application, hereby claim the priority date under the International Convention of the following Korean application:

Appln. No. 1998-10584 filed: March 26, 1998

as acknowledged in the Declaration of the subject application.

A certified copy of said application is being submitted herewith.

Respectfully submitted,

JONES, VOLENTINE, STEINBERG & WHITT, L.L.P.

By: _____
Brian C. Altmiller
Registration No. 37,271

BCA:tmd

JONES, VOLENTINE, STEINBERG & WHITT, L.L.P.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Tel. (703) 715-0870

Dated: March 26, 1999

SEC.506

METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT

This application relies for priority upon Korean Patent Application No. 98-10584, filed on March 26, 1998, the contents of which are herein incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a method for manufacturing a capacitor. More particularly, the present invention relates to a method for manufacturing a capacitor having a dielectric layer with a high dielectric constant, i.e., having a high dielectric layer.

As the integration of a dynamic random access memory (DRAM) semiconductor device increases, the area that may used for a capacitor is reduced within a defined cell area. This reduction in available capacitor area makes it difficult to obtain the capacitance required for the operation of a semiconductor device using conventional dielectric layers such as an oxide layer and a nitride layer.

In order to increase capacitance, several methods have been proposed for forming a storage electrode of a capacitor using a three-dimensional structure. However, even when a three-dimensional storage electrode is used, it is still difficult to obtain the capacitances required for a highly integrated semiconductor devices using conventional dielectric layer materials.

SEC.506

To solve the above problems, a method has been proposed that uses a high dielectric layer, e.g., a $(Ba,Sr)TiO_3$ or 'BST' layer, for the capacitor of the semiconductor device. However, if a high dielectric layer is employed for the capacitor, a noble metal electrode must be used as the plate and storage electrodes in order to obtain a high capacitance by suppressing the reaction of the high dielectric layer with the plate and storage nodes during subsequent processes. Furthermore, the noble metal electrode has strong reaction with silicon, so a barrier layer must be formed between the noble metal electrode and the high dielectric layer. However, when this is done, the barrier layer may be oxidized during a subsequent process, which can short an electrode or increase the leakage current.

SUMMARY OF THE INVENTION

To solve the above problems, it is an objective of the present invention to provide a method for manufacturing a capacitor in a semiconductor device in which a barrier layer is prevented from being oxidized and the leakage current is reduced when a high dielectric layer is employed for the capacitor.

In order to achieve these objectives, a method is provided for manufacturing a capacitor of a semiconductor device, comprising: forming a storage electrode over a semiconductor substrate, forming a high dielectric layer over the storage electrode, forming a plate electrode over the high dielectric layer, performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature, and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

This method may further comprise forming an interdielectric layer over the plate electrode, or performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.

The first and second post-annealings may be performed in sequence after forming a high dielectric layer, after forming a plate electrode, or after forming an interdielectric layer. The first and second post-annealings may also be separated, for example, the first post-annealing step being performed after forming the high dielectric layer, and the second post-annealing step being performed after forming the plate electrode.

There is also provided a method of manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode and an interdielectric layer are in sequence formed on a semiconductor substrate, includes the steps of performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature, e.g., about 600°C to 900°C, after forming the high dielectric layer, the plate electrode or the interdielectric layer; and then performing a second post-annealing of the semiconductor substrate post-annealed at a second temperature lower than the first temperature, e.g., about 100°C to 600°C.

Also, a method for manufacturing a capacitor of a semiconductor device, in which a storage electrode, a high dielectric layer, a plate electrode and an interdielectric layer are in sequence formed on a semiconductor substrate, includes the steps of: post-

annealing the semiconductor substrate where the high dielectric layer is formed, under an inert atmosphere at a first temperature, e.g., 600 ~ 900°C; and then post-annealing the semiconductor substrate post-annealed at a second temperature lower than the first temperature, e.g., 100 ~ 600°C, after forming the plate electrode.

The high dielectric layer may be formed of a dielectric material having a Perovskite such as (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, or (Pb, La)(ZrTi)O_3. The plate electrode and the storage electrode may be formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir. The post-annealing at the first and second temperatures may be performed separately or in the same location. Also, the post-annealing at the first and second temperatures may be performed in a furnace or a rapid vacuum thermal annealing apparatus.

According to a method for manufacturing a capacitor of a semiconductor device of the present invention, the first post-annealing is performed under an inert atmosphere at a high temperature after depositing a high dielectric layer, forming a plate electrode or an interdielectric layer, and then the second post-annealing is performed at a lower temperature, after the first post-annealing. The first and second post annealing steps can be performed after the deposition of the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination of this, so long as the second post-annealing is performed after the first post-annealing. The two post-annealings do not have to be performed in the same place or at the same stage during the fabrication process. As a

result of this process, the dielectric constant of the high dielectric layer is increased and the oxidation of a barrier layer is suppressed, which acts to reduce the leakage current.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objective and advantages of the present invention will become more apparent by describing in detail a preferred embodiment of the present invention with reference to the attached drawings in which:

Figs. 1 through 5 are sectional views illustrating a method for manufacturing a capacitor of a semiconductor device according to a first preferred embodiment of the present invention;

Fig. 6 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to the first preferred embodiment of the present invention;

Fig. 7 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a second preferred embodiment of the present invention;

Fig. 8 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a third preferred embodiment of the present invention;

Fig. 9 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a fourth preferred embodiment of the present invention;

SEC.506

Fig. 10 is a graph illustrating the capacitance of a capacitor of a semiconductor device formed by a conventional post-annealing method;

Fig. 11 is a graph illustrating the capacitance of a capacitor of a semiconductor device formed by a post-annealing method according to preferred embodiments of the present invention;

Fig. 12 is a graph illustrating leakage current characteristics of a capacitor of a semiconductor device formed by a post-annealing method according to preferred embodiments of the present invention; and

Fig. 13 is a graph illustrating leakage current characteristics of a capacitor of a semiconductor device formed according to preferred embodiments of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1 through 5 are sectional views illustrating a method for manufacturing a capacitor of a semiconductor device having a high dielectric layer according to a first preferred embodiment of the present invention. Fig. 6 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to the first preferred embodiment of the present invention. While the process is described below with respect to Figs. 1 to 5, the corresponding steps shown in Fig. 6 will be given in parenthesis, where appropriate.

SEC.506

As shown in Fig. 1, a first interdielectric layer 3 having one or more contact holes 2 is formed over a semiconductor substrate 1, e.g., a silicon substrate, where a transistor (not shown) is formed (Step 100). The contact holes 2 are formed such that a predetermined portion of the semiconductor substrate 1, e.g., a source region of the transistor, is exposed. Although more than one contact hole may be formed, for ease of explanation, the following description will only describe a single contact hole. It should be understood, however, that the process would be similar for multiple contact holes.

Referring to Fig. 2, a polysilicon layer doped with an impurity such as phosphorus is deposited over the entire surface of the semiconductor substrate 1 where the contact hole 2 is formed, filling the contact hole 2. The resultant structure is then chemically/mechanically polished to form a burial layer 5 in the contact hole 2. Then, a metal layer, e.g., titanium, is deposited over the entire surface of a substrate where the burial layer 5 and the first interdielectric layer 3 are formed, and the resultant structure, including the metal layer, is annealed and etched to selectively form a metal silicide 7 over the burial layer 5. By this process, a plug 8 is formed in the contact hole 2, the plug being made up of the burial layer 5 and the metal silicide 7 (Step 105).

Referring to Fig. 3, a barrier layer 9 is formed over the entire surface of the semiconductor substrate 1 where the plug 8 is formed. The barrier layer 9 prevents the silicon of the plug from reacting with a first conductive layer 11, which is used to form a storage electrode. The barrier layer 9 is preferably formed of Ti, TiN, TiAlN, TiSiN, TaN, TaAlN, or TaSiN.

SEC.506

The first conductive layer 11, which will be used as a storage electrode of a capacitor in a semiconductor device, is then formed over the barrier layer 9 (Step 110). The first conductive layer 11 is preferably formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir. This is because the non-oxidative metal used for the first conductive layer is an inert material that prevents the first conductive layer 11 from being oxidized when a high dielectric layer is formed at a high temperature. A mask pattern 13 that is used as an oxide layer is then formed over the first conductive layer 11 for the storage electrode.

Referring to Fig. 4, the first conductive layer 11 and the barrier layer 9 are plasma-etched using the mask pattern 13 as a mask, thereby forming a barrier layer pattern 9a and a first conductive layer pattern 11a. The barrier layer pattern 9a and the first conductive layer pattern 11a become a storage electrode 14 of the capacitor (Step 115).

As shown in Fig. 5, the mask pattern 13 is removed and a high dielectric layer 15 is formed over the entire surface of the semiconductor substrate 1 where the storage electrode is formed. Preferably the high dielectric layer is formed by sputtering at about 400 ~ 510°C to a height of about 400 ~ 500Å (Step 120). The high dielectric layer 15 preferably comprises a dielectric material having a Perovskite structure, such as (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3 or (Pb, La)(ZrTi)O_3.

In order to obtain high capacitance and low leakage current from the manufactured capacitor, the semiconductor substrate over which the high dielectric layer 15 is formed is

then post-annealed (Step 125). Preferably, the semiconductor substrate 1 over which the high dielectric layer 15 is formed is post annealed in multiple annealing steps. In the case where two annealing steps are used, the semiconductor substrate is initially post-annealed in a first post-annealing step at a first temperature, e.g., 600 ~ 900°C. This first post-annealing at the first temperature is preferably performed under an inert atmosphere, e.g., under a nitrogen atmosphere of 100ppm of oxygen or less, in a furnace or a rapid vacuum thermal annealing apparatus. Then, the semiconductor substrate 1 is again post-annealed in a second post annealing step, preferably in an oxygen atmosphere at a second temperature lower than the first temperature, e.g., 100 ~ 600°C. This second post-annealing step is also preferably performed in a furnace or a rapid vacuum thermal annealing apparatus. The first and second post-annealing steps may be performed separately or *in-situ*.

In addition, although a two step post-annealing process is described by way of example, it should be understood that the post-annealing may also be performed in multiple steps at three or more temperatures. For example, in a three step post annealing process, the three temperatures used would be a first temperature, a second temperature lower than the first temperature, and a third temperature lower than the second temperature.

Referring again to Fig. 5, after the formation of the high dielectric layer 15, a second conductive layer 17, to be used for a plate electrode, is formed over the high dielectric layer 15, to complete a capacitor (Step 130). The second conductive layer 17

for the plate electrode is preferably formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir.

Subsequently, a second interdielectric layer 19 is formed over the entire surface of the semiconductor substrate 1 where the plate electrode 17 is formed (Step 135). Additional processes may then be performed in the same manner as with the manufacturing of conventional semiconductor devices.

Fig. 7 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a second preferred embodiment of the present invention.

The same reference numerals as those of Figs. 1 through 6 represent the same elements. The second embodiment of the present invention is the same as the first embodiment, except that, the multiple-steps post -annealing is performed after, rather than before, the step of forming the plate electrode. In detail, steps 100 ~ 120 shown in Figs. 1 through 5 of the first embodiment are performed on the semiconductor substrate 1 to form the same storage electrode and high dielectric layer 15 as in the first embodiment. As in the first preferred embodiment, the high dielectric layer 15 is preferably formed of a dielectric material having a Perovskite structure such as (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3 or (Pb, La)(ZrTi)O_3.

A plate electrode 17 is then formed in the same manner as described in Step 130 of the first embodiment, over the high dielectric layer 15 (Step 140). As in the first

preferred embodiment, the plate electrode 17 is preferably formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir.

In order to obtain a high capacitance and a low leakage current from the capacitor, the semiconductor substrate 1 over which the plate electrode 17 is formed is post-annealed in multiple steps (Step 145). In the second preferred embodiment, a two-step post-annealing process is used.

In detail, the semiconductor substrate 1 is initially post-annealed in a first post-annealing step at a first temperature, e.g., 600 ~ 900°C. The first post-annealing step is preferably performed under an inert atmosphere, e.g., a nitrogen atmosphere having fewer than 100ppm of oxygen, in a furnace or a rapid vacuum thermal annealing apparatus. Then, the semiconductor substrate 1 is again post-annealed in a second post-annealing step at a second temperature lower than the first temperature, e.g., 100 ~ 600°C. The second post-annealing step is preferably performed in a furnace or a rapid vacuum thermal annealing apparatus. The first and second post-annealing steps may performed separately or *in-situ*.

In addition, although a two step post-annealing process is described by way of example, it should be understood that the post-annealing may also be performed in multiple steps at three or more temperatures, as long as the temperatures gradually decrease. For example, in a three step post annealing process, the three temperatures used

would be a first temperature, a second temperature lower than the first temperature, and a third temperature lower than the second temperature.

Subsequently, a second interdielectric layer 19 is formed over the entire surface of the semiconductor substrate where the storage electrode 14, the high dielectric layer 15 and the plate electrode 17 are formed (Step 150). Additional processes may then be performed in the same manner as in a typical method for manufacturing a semiconductor device.

Fig. 8 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a third preferred embodiment of the present invention. The same reference numerals as those of Figs. 1 through 6 represent the same elements. The third preferred embodiment of the present invention is the same as the second preferred embodiment, except that the multiple annealing steps are performed after step of forming a second interdielectric layer.

In detail, the storage electrode, high dielectric layer 15, and plate electrode 140 are formed over the semiconductor substrate 1 in the same manner as described with reference to steps 100 through 140 of Figs. 1 through 5 and Fig. 7 of the second preferred embodiment. The high dielectric layer 15 is preferably formed of a dielectric material having a Perovskite structure, such as (Sr, Ti)O_3, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, or (Pb, La)(ZrTi)O_3, and the plate electrode 17 is preferably formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir.

SEC.506

Subsequently, a second interdielectric layer 19 is formed over the entire surface of the semiconductor substrate over which the plate electrode 17 is formed (Step 160).

In order to obtain high capacitance and low leakage current of the capacitor, the semiconductor substrate 1 over which the second interdielectric layer 19 is formed is then post-annealed in a multiple-step post-annealing process (Step 165). In the third preferred embodiment, a two-step post-annealing process is used.

In detail, the semiconductor substrate 1 over which the second interdielectric layer 19 is formed is initially post-annealed in a first post-annealing step at a first temperature, e.g., 600 ~ 900°C. The first post-annealing step is preferably performed under an inert atmosphere, e.g., a nitrogen atmosphere having 100ppm of oxygen or less, in a furnace or a rapid vacuum thermal annealing apparatus. Then, the primary post-annealed semiconductor substrate is again post-annealed in a second post annealing step at a second temperature lower than the first temperature, e.g., 100 ~ 600°C. The second post-annealing step is preferably performed under an atmosphere of oxygen in a furnace or a rapid vacuum thermal annealing apparatus. The first and second post-annealing steps may be performed separately or *in-situ*.

In addition, although a two step post-annealing process is described by way of example, it should be understood that the post-annealing may also be performed in multiple steps at three or more temperatures, as long as the temperatures gradually decrease. For example, in a three step post annealing process, the three temperatures used

would be a first temperature, a second temperature lower than the first temperature, and a third temperature lower than the second temperature.

Fig. 9 is a flowchart illustrating a method for manufacturing a capacitor of a semiconductor device according to a fourth preferred embodiment of the present invention. The same reference numerals as those of Figs. 1 through 6 of the first embodiment represent the same elements. The fourth preferred embodiment of the present invention is the same as the first preferred embodiment, except that a first post-annealing step is performed at a first temperature after the step of forming a high dielectric layer, and then a second post-annealing step is performed at a second temperature after the step of forming a plate electrode.

In detail, a storage electrode 14 and a high dielectric layer 15 are formed over a semiconductor substrate in the same manner as in steps 100 through 120 of Figs. 1 through 4 of the first preferred embodiment (Step 120). Then, the semiconductor substrate 1, where the high dielectric layer 15 is formed, is initially post-annealed in a first post-annealing step at a first temperature, e.g., 600 ~ 900°C (step 170). The first post-annealing step is preferably performed under an inert atmosphere, e.g., a nitrogen atmosphere having 100ppm of oxygen or less, preferably in a furnace or a rapid vacuum annealing apparatus.

A plate electrode 17 is then formed over the high dielectric layer 15 in the same manner as described in Step 130 of the first embodiment (Step 175). The high dielectric layer 15 is preferably formed of Pt, Ru, Ir, IrO_2, RuO_2, a conductive material having a

Perovskite structure such as $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, or an alloy containing Ir.

After the plate electrode 17 is formed, the semiconductor substrate 1 is again post-annealed in a second post-annealing step, preferably under an oxygen atmosphere at a second temperature lower than the first temperature, e.g., 100 ~ 600°C (step 180). The post-annealing at the second temperature is preferably performed in a furnace or a rapid vacuum annealing apparatus.

In addition, although a split two step post-annealing process is described by way of example, it should be understood that the post-annealing may also be performed in multiple steps at three or more temperatures, as long as the temperatures gradually decrease. For example, in a three step post annealing process, the three temperatures used would be a first temperature, a second temperature lower than the first temperature, and a third temperature lower than the second temperature. In this embodiment, the various post-annealing steps would be split up sequentially such that one or more took place after the step of forming a high dielectric layer (Step 120) and one or more took place after the step of forming a plate electrode (Step 175).

Subsequently, a second interdielectric layer 19 is formed over the entire surface of the semiconductor substrate 1 where the plate electrode 17 is formed (Step 185). Additional processes may then be performed in the same manner as in a typical method for manufacturing a semiconductor device.

SEC.506

In order to manufacture a capacitor of a semiconductor device according to the first preferred embodiment of the present invention, capacitance and leakage current are described as follows.

Fig. 10 is a graph illustrating the capacitance of a capacitor of a semiconductor device formed according to a related annealing method.

In detail, Fig. 10 shows the capacitance per cell of a capacitor having a high dielectric BST layer deposited at 400°C to a thickness of 400Å. Reference character **a** represents the capacitance after forming a plate electrode; reference character **b** represents the capacitance after post-annealing in a furnace of 550°C under an oxygen atmosphere; and reference character **c** represents the capacitance after post-annealing in a furnace of 650°C under an oxygen atmosphere.

In detail, the capacitance **a** of the capacitor after forming the plate electrode is approximately 5fF/cell, and the capacitance **b** after post-annealing under the oxygen atmosphere is increased to 16.5fF/cell. However, the capacitance **c** after post-annealing under the oxygen atmosphere of 650°C is 1fF/cell or less due to the oxidation of the barrier layer, so that advantageous properties of the high dielectric layer capacitor are not realized.

As shown by this example, post-annealing at a temperature in which the barrier layer is not oxidized increases the capacitance to a predetermined degree, but post annealing at a temperature at which the barrier layer is oxidized, reduces the capacitance due to the oxidation of the barrier layer. Thus, in order to use the high dielectric layer for

the capacitor, it is necessary to anneal at a high temperature while suppressing oxidation of the barrier layer.

Fig. 11 is a graph illustrating the capacitance of a capacitor of a semiconductor device using a post-annealing process in accordance with preferred embodiments of the present invention.

In detail, Fig. 11 shows the capacitance per cell of a capacitor having a high dielectric BST layer deposited at 450°C to a thickness of 400Å. Here, reference character **a** represents the capacitance after forming the plate electrode; reference character **b** represents the capacitance after a post-annealing in a furnace of 700°C under a nitrogen atmosphere having 100ppm of oxygen of or less; and reference character **c** represents the capacitance after a first post-annealing step in a furnace of 700°C under a nitrogen atmosphere, and then a second post-annealing step in a furnace of 400°C containing oxygen.

In detail, the deposition temperature of the BST layer of Fig. 11 is higher than that of the capacitor of Fig. 10, so that the capacitance **a** after forming the plate electrode is higher than that of Fig. 10, at 7.5fF/cell. Also, the capacitance **b** of the capacitor after the first post-annealing step under the nitrogen atmosphere including little or no oxygen has a value of 21fF/cell. As described above, in order to obtain the high capacitance during a process in which the BST layer is used in the capacitor, the post-annealing must be performed under an atmosphere in which the barrier layer is not oxidized.

SEC.506

However, if the capacitor is post-annealed at a high temperature as with reference character **b**, the capacitance is increased, but the leakage current is increased as shown in Fig. 12, resulting in an unreliable capacitance. The increase in the leakage current is caused by stress mismatching due to a stress change between the BST layer and the plate and storage electrodes during the annealing at a high temperature.

In order to solve the stress mismatching, a multiple-step annealing process, i.e., a first annealing step at a high temperature under a nitrogen atmosphere and then a second annealing step at a low temperature, was performed. In other words, as represented by reference character **c**, a first post-annealing step was performed under a nitrogen atmosphere at 700°C, and then a second post-annealing step was performed under an oxygen atmosphere at 400°C. The capacitance **c** of the capacitor after the multiple-step annealing process is 21fF/cell, similar to the capacitance **b**. From this result, the capacitance of a capacitor fabricated by a multiple step annealing process does not change significantly. Also, after the multiple annealing steps, the leakage current was reduced by an order of 5 ~ 6 on the basis of 1V as shown in Fig. 12.

Fig. 12 is a graph illustrating the leakage current of a capacitor of a semiconductor device according to the post-annealing steps of preferred embodiments of the present invention.

In detail, Fig. 12 shows the leakage current of the capacitor after post-annealing of the manufactured capacitor. In particular, reference character **a** represents the capacitance after post-annealing at 700°C, and reference character **b** represents the

capacitance after a multiple-step post-annealing, including a first post-annealing step in a furnace at 700°C under a nitrogen atmosphere and then a second post-annealing step in a furnace containing oxygen at 400°C. The leakage current after post-annealing, as shown by plot **b**, is reduced by 5 ~ 6 orders of magnitude on the basis of 1V, compared with the capacitance **a** after a single post-annealing step under a nitrogen atmosphere at a high temperature.

Fig. 13 is a graph illustrating the leakage current of a capacitor of a semiconductor device according to preferred embodiments of the present invention.

In detail, Fig. 13 shows the leakage current of the capacitor after forming a second interdielectric layer and then post-annealing. Reference character **a** represents the capacitance of a capacitor post-annealed under a nitrogen atmosphere at 650°C, and reference character **b** represents the capacitance of a capacitor post-annealed in a multiple post annealing process, including a first post-annealing step in a furnace under a nitrogen atmosphere at 650°C and a second post annealing step in a furnace containing oxygen at 400°C.

In detail, in plot **b** of the capacitor is post-annealed in a multiple-step post-annealing process after depositing the second interdielectric layer. In this case, the leakage current is reduced compared with the plot **a** of a capacitor post-annealed in a single step under a nitrogen atmosphere.

According to the method for manufacturing a capacitor of a semiconductor device of the present invention, a multiple step post-annealing process is performed in which a

first post-annealing step is performed under an inert atmosphere at a high temperature after depositing a high dielectric layer, forming a plate electrode or an interdielectric layer, and second post-annealing step is performed at a low temperature; or a first post-annealing step is performed under an inert gas at a high temperature after depositing the high dielectric layer and a second post-annealing step is performed after forming the plate electrode, so that the dielectric constant of the high dielectric layer is increased and the oxidation of a barrier layer is suppressed, to reduce leakage current.

It should be understood that the invention is not limited to the illustrated embodiments and that many changes and modifications can be made within the scope of the invention by a person skilled in the art.

SEC.506

What is claimed is:

1. A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

2. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the high dielectric layer comprises a material selected from the group consisting of $(Sr, Ti)O_3$, $(Ba, Sr)TiO_3$, $Pb(Zr, Ti)O_3$, and $(Pb, La)(ZrTi)O_3$.

3. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the plate electrode and the storage electrode comprises a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

4. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first temperature is between 600°C and 900°C.

5. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the second temperature is between 100°C and 600°C.

6. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed separately or in-situ.

7. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed in a furnace or a rapid vacuum thermal annealing apparatus.

8. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the high dielectric layer.

9. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first and second post-annealing steps are performed after the step of forming the plate electrode.

10. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

11. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising forming an interdielectric layer over the plate electrode.

12. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first and second post-annealing steps are performed after the step of forming the interdielectric layer.

13. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 11, wherein the first post-annealing step is performed after the step of forming the high dielectric layer and the second post-annealing step is performed after the step of forming the plate electrode.

14. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 1, further comprising performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.

15. A method for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature, after forming one of the high dielectric layer, the plate electrode, and the interdielectric layer; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature.

16. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the high dielectric layer comprises a material selected from the group consisting of $(Sr, Ti)O_3$, $(Ba, Sr)TiO_3$, $Pb(Zr, Ti)O_3$, and $(Pb, La)(ZrTi)O_3$.

17. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the plate electrode and the storage electrode comprise a material selected from the group consisting of Pt, Ru, Ir, IrO_2, RuO_2, $SrRuO_3$, $CaSrRuO_3$, $BaSrRuO_3$, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

18. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the first temperature is between 600°C and 900°C.

19. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, wherein the second temperature is between 100°C and 600°C.

20. A method for manufacturing a capacitor of a semiconductor device, as recited in claim 15, further comprising performing a third post-annealing, after the second post-annealing, at a third temperature lower than the second temperature.

SEC.506

Abstract of the Disclosure

A method is provided for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed over a semiconductor substrate. This method includes the steps of performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature and then performing a second post-annealing of the semiconductor substrate at a second temperature. The first and second post annealing steps can be performed after the deposition of the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination of this, so long as the second post-annealing step is performed after the first post-annealing step. The two post-annealing steps do not have to be performed in the same place or at the same stage during the fabrication process. The first temperature is preferably in the range of about 600°C to 900°C, and the second temperature is preferably in the range of about 100°C to 600°C. In this way, the dielectric constant of the high dielectric layer is increased, and the leakage current is reduced.

FIG. 1

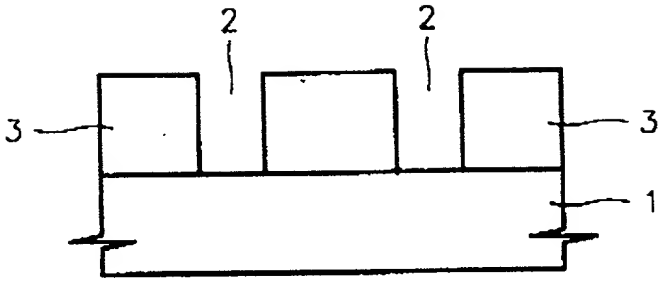


FIG. 2

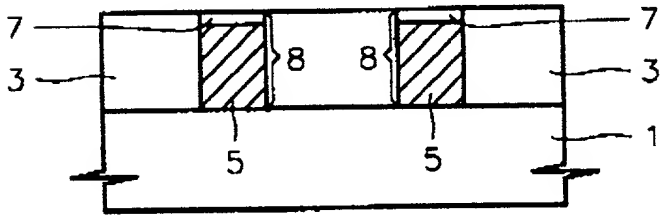


FIG. 3

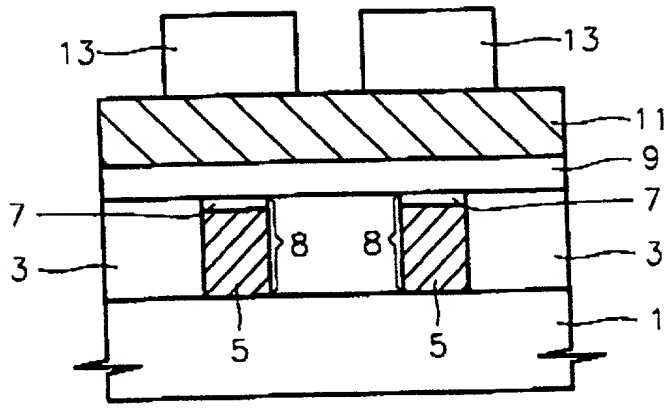


FIG. 4

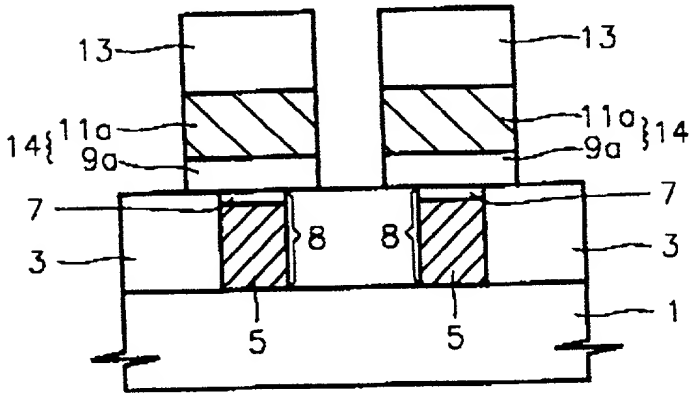


FIG. 5

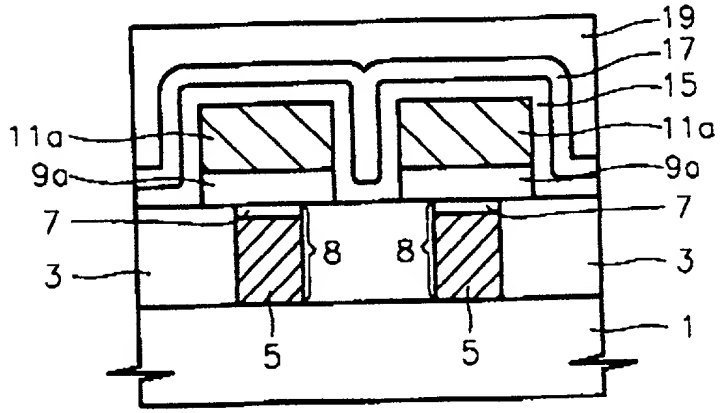


FIG. 6

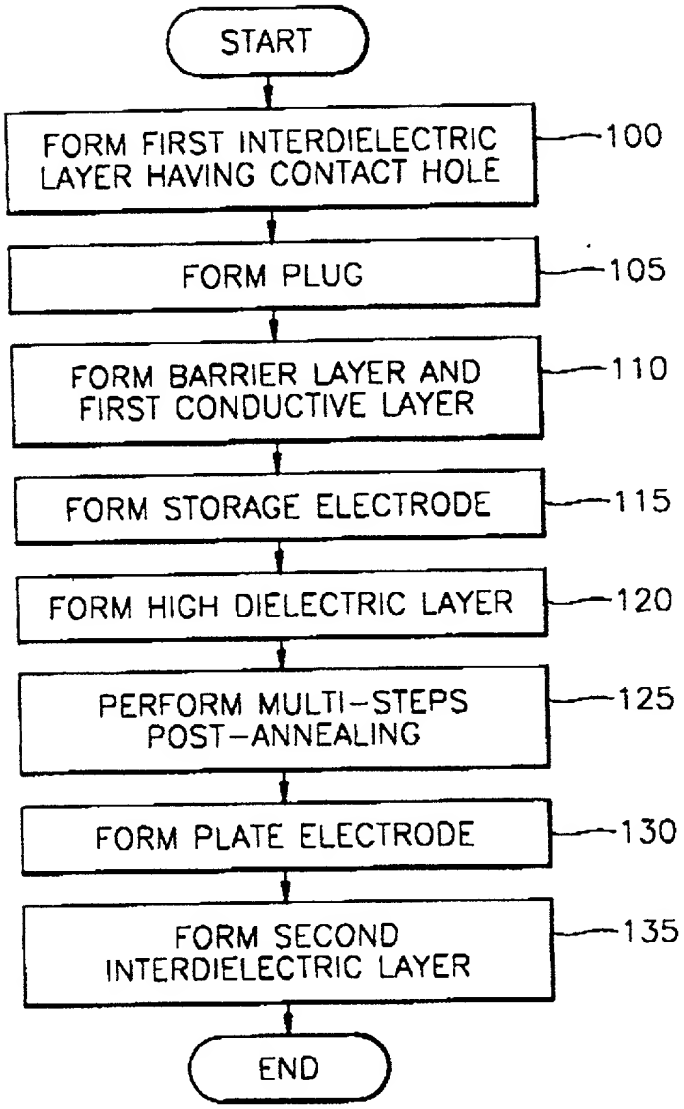

START
FORM FIRST INTERDIELECTRIC LAYER HAVING CONTACT HOLE
100
FORM PLUG
105
FORM BARRIER LAYER AND FIRST CONDUCTIVE LAYER
110
FORM STORAGE ELECTRODE
115
FORM HIGH DIELECTRIC LAYER
120
PERFORM MULTI-STEPS POST-ANNEALING
125
FORM PLATE ELECTRODE
130
FORM SECOND INTERDIELECTRIC LAYER
135
END

FIG. 7

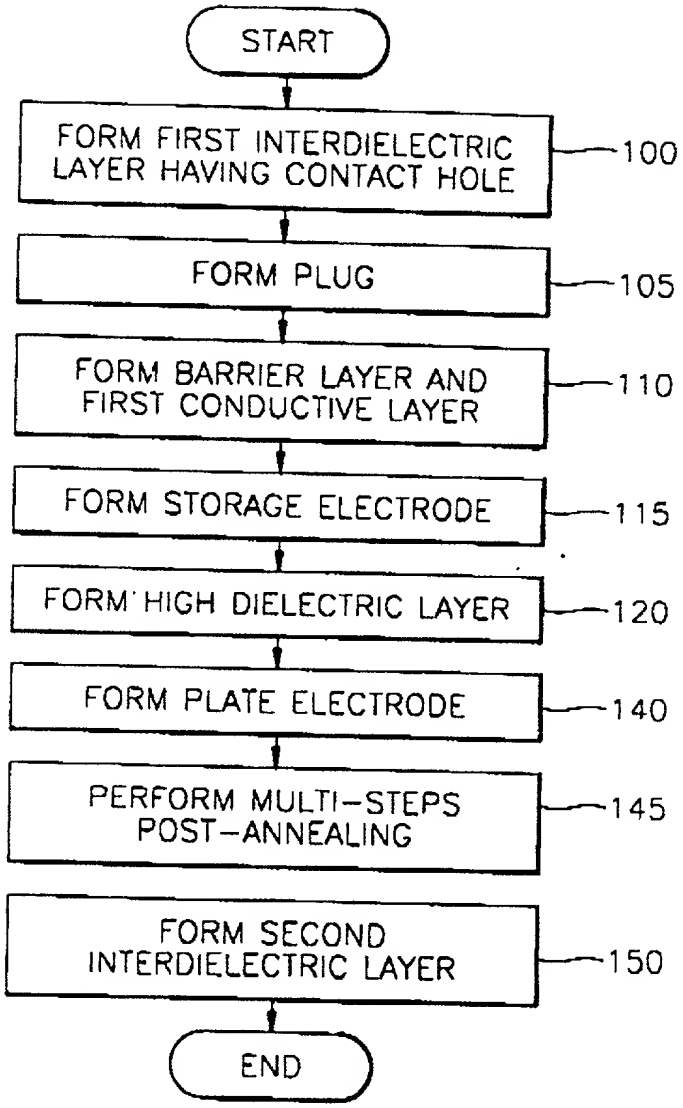

START
FORM FIRST INTERDIELECTRIC LAYER HAVING CONTACT HOLE
100
FORM PLUG
105
FORM BARRIER LAYER AND FIRST CONDUCTIVE LAYER
110
FORM STORAGE ELECTRODE
115
FORM HIGH DIELECTRIC LAYER
120
FORM PLATE ELECTRODE
140
PERFORM MULTI-STEPS POST-ANNEALING
145
FORM SECOND INTERDIELECTRIC LAYER
150
END

FIG. 8

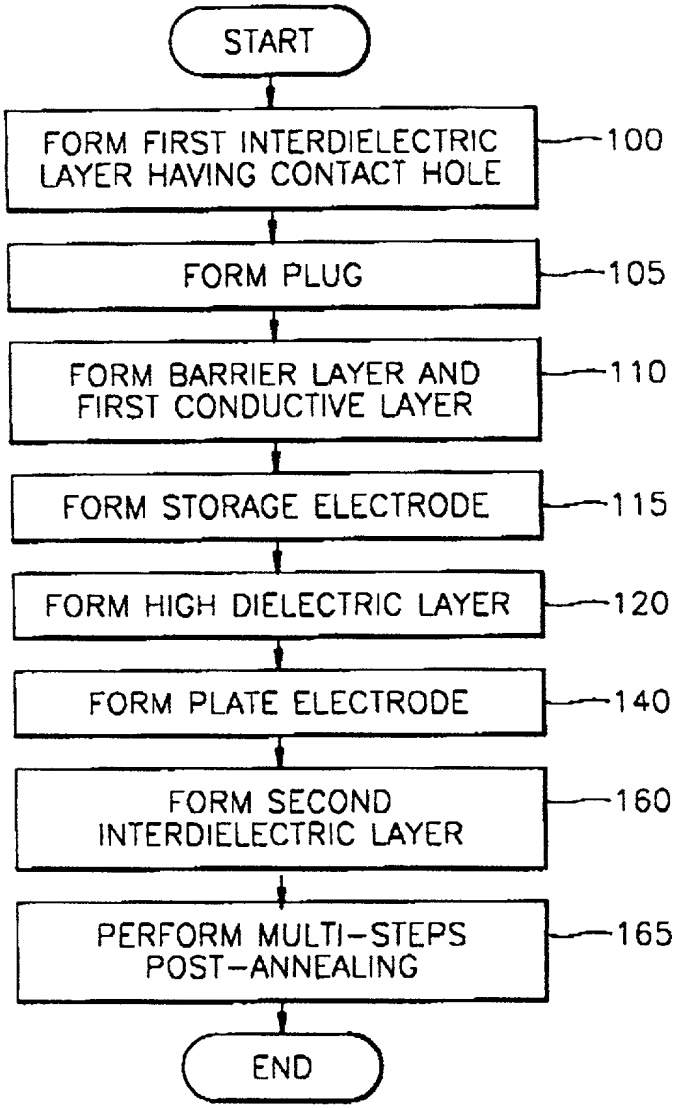

START
FORM FIRST INTERDIELECTRIC LAYER HAVING CONTACT HOLE
100
FORM PLUG
105
FORM BARRIER LAYER AND FIRST CONDUCTIVE LAYER
110
FORM STORAGE ELECTRODE
115
FORM HIGH DIELECTRIC LAYER
120
FORM PLATE ELECTRODE
140
FORM SECOND INTERDIELECTRIC LAYER
160
PERFORM MULTI-STEPS POST-ANNEALING
165
END

FIG. 9

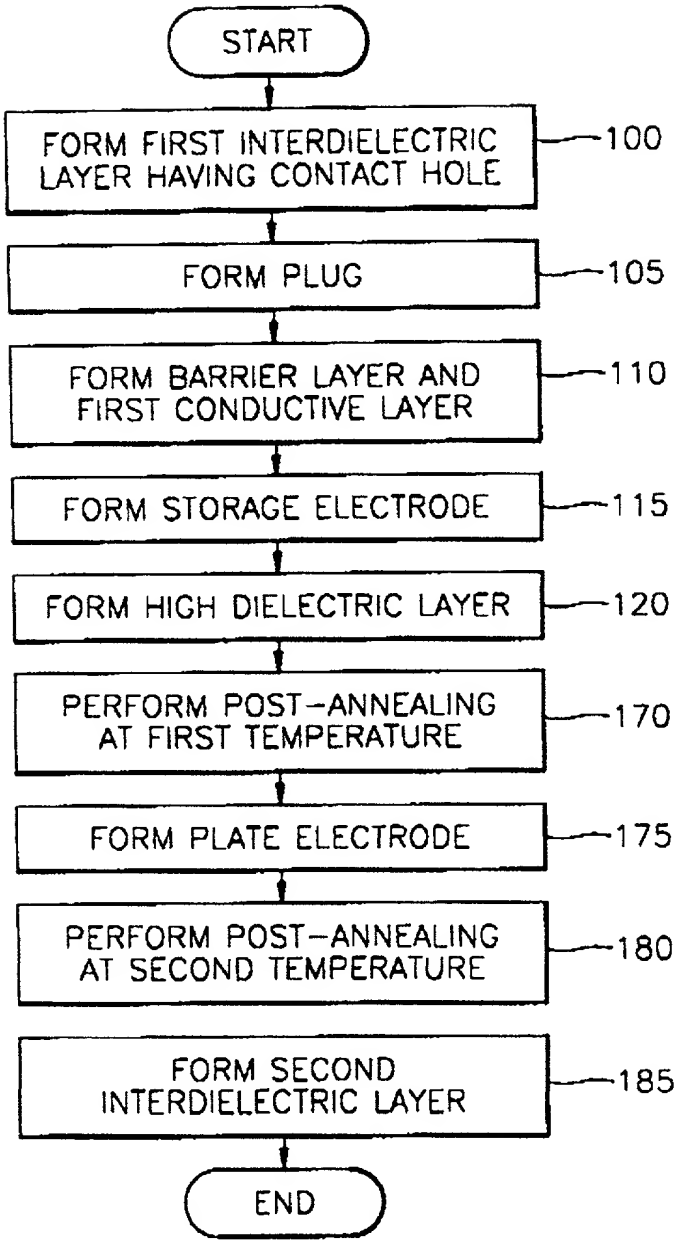

START
FORM FIRST INTERDIELECTRIC LAYER HAVING CONTACT HOLE
100
FORM PLUG
105
FORM BARRIER LAYER AND FIRST CONDUCTIVE LAYER
110
FORM STORAGE ELECTRODE
115
FORM HIGH DIELECTRIC LAYER
120
PERFORM POST-ANNEALING AT FIRST TEMPERATURE
170
FORM PLATE ELECTRODE
175
PERFORM POST-ANNEALING AT SECOND TEMPERATURE
180
FORM SECOND INTERDIELECTRIC LAYER
185
END

FIG. 10

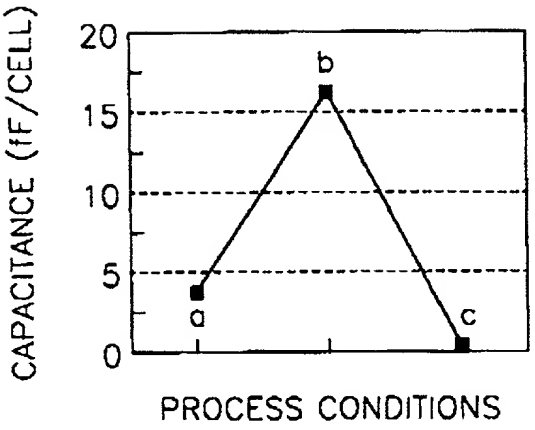

CAPACITANCE (fF/CELL)
20
15
10
5
0
a
b
c
PROCESS CONDITIONS

FIG. 11

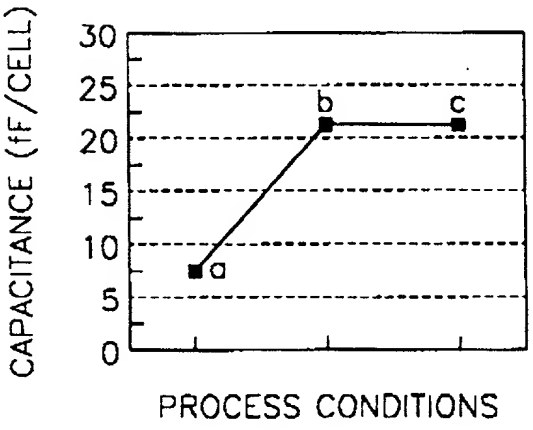

CAPACITANCE (fF/CELL)
30
25
20
15
10
5
0
a
b
c
PROCESS CONDITIONS

FIG. 12

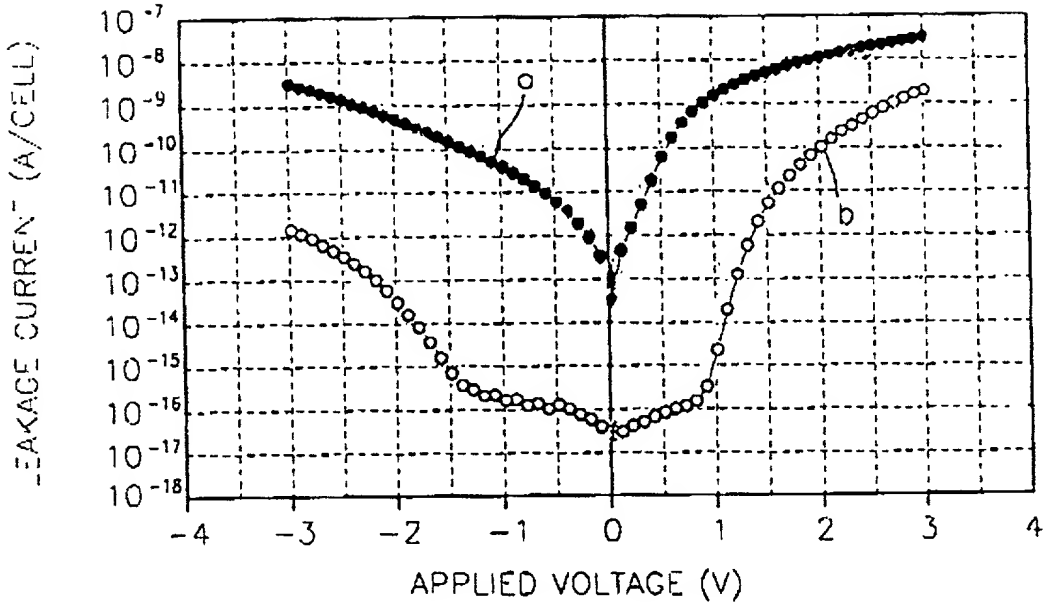
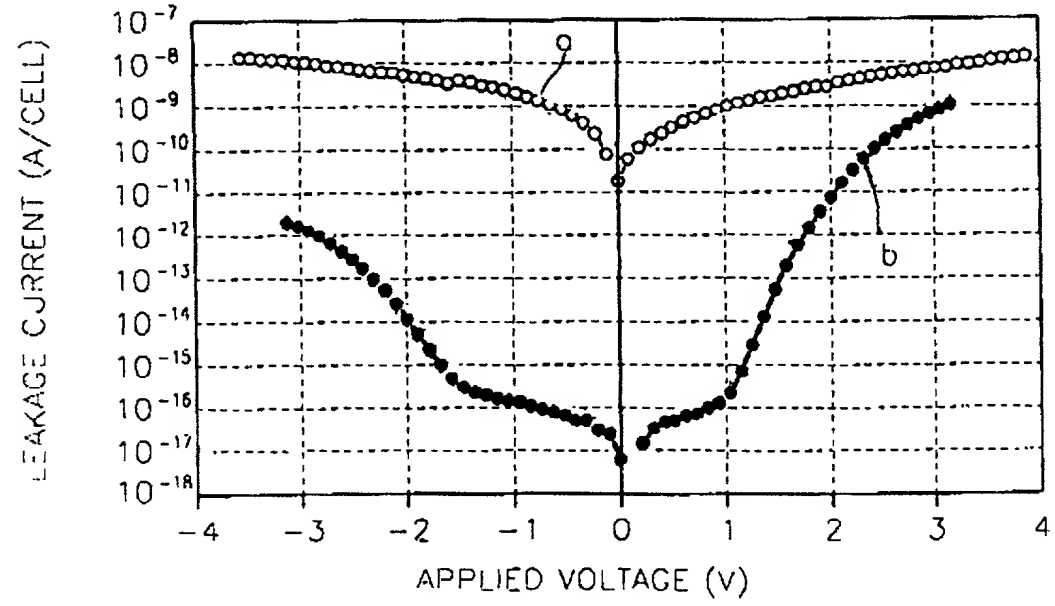

LEAKAGE CURRENT (A/CELL)
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
10^{-16}
10^{-17}
10^{-18}
a
b
−4 −3 −2 −1 0 1 2 3 4
APPLIED VOLTAGE (V)

FIG. 13


LEAKAGE CURRENT (A/CELL)
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
10^{-16}
10^{-17}
10^{-18}
a
b
−4 −3 −2 −1 0 1 2 3 4
APPLIED VOLTAGE (V)

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(x) Original ( ) Supplemental ( ) Substitute ( ) PCT ( ) Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT
of which is described and claimed in:

(x) the attached specification, *or*

( ) the specification in the application Serial No._____ filed_____,

and with amendments through_____ (if applicable), *or*

( ) the specification in International Application No. PCT/_____, filed _____,

and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the content of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (and §172 if this application is for a Design) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
KOREA	98-10584	March 26, 1998	X

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

And I hereby appoint Raymond C. Jones, Reg. No. 34,631, Adam C. Volentine, Reg. No. 33,289, Neil A. Steinberg, Reg. No. 34,735, and Stephen R. Whitt, Reg. No. 34,753, members of the firm of JONES, VOLENTINE, STEINBERG & WHITT, L.L.P., jointly and severally, attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from Y.P. LEE AND ASSOCIATES as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and myself. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys named herein will be so notified by me.

Kindly direct all correspondence to: **JONES, VOLENTINE, STEINBERG & WHITT, L.L.P.**
12200 Sunrise Valley Drive
Suite 150
Reston, Virginia 20191

Telephone (703) 715-0870

Full Name of 1st Inventor	FAMILY NAME LEE	FIRST GIVEN NAME Byoung-taek	SECOND GIVEN NAME
Residence & Citizenship	CITY Seoul	STATE OR COUNTRY Republic of Korea	COUNTRY OF CITIZENSHIP Republic of Korea
Post Office Address	ADDRESS 101-1105, Hyundai Kwanak Apt., 1000 Bongcheon-dong, Kwanak-gu, Seoul, Republic of Korea	CITY	STATE OR COUNTRY / ZIP CODE

Full Name of 2nd Inventor	FAMILY NAME LEE	FIRST GIVEN NAME Ki-hoon	SECOND GIVEN NAME
Residence & Citizenship	CITY Kyungki-do	STATE OR COUNTRY Republic of Korea	COUNTRY OF CITIZENSHIP Republic of Korea
Post Office Address	ADDRESS 107-1005, Pungrim Apt., Pungdeokcheon-ri, Suji-eub, Yongin-city, Kyungki-do, Republic of Korea	CITY	STATE OR COUNTRY / ZIP CODE

Full Name of 3rd Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY / ZIP CODE

Full Name of 4th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

Full Name of 5th Inventor	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME	
Residence & Citizenship	CITY	STATE OR COUNTRY	COUNTRY OF CITIZENSHIP	
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true, and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1st Inventor ______________________________ Date ____________
Byoung-taek LEE

2nd Inventor ______________________________ Date ____________
Ki-hoon LEE

3rd Inventor ______________________________ Date ____________

4th Inventor ______________________________ Date ____________

5th Inventor ______________________________ Date ____________

* *

Applicant Reference No.: SS-11644-US Atty Docket No.: SEC.506